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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,508	07/29/2003	Jordan Plofsky	ALTRP082	6910

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EXAMINER
IQBAL, NADEEM

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,508	PLOFSKY, JORDAN	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

NADEEM IQBAL
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Apr 28,06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an amendment filed on July 19, 2006.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson (U.S. Patent number 7020598).

3. As per claim 1, Jacobson teaches (col. 3, lines 38-40) a diagnostic microcontroller that initiates diagnostic testes on the programmable logic device (See Fig. 1) . He thus teaches a programmable logic device comprising a programmable logic that includes test logic, a port, and a hard-coded microprocessor in communication with the programmable logic. He also teaches (col. 3, lines 50-53) diagnostic microcontroller initiates diagnostic tests on the programmable logic device to test its functionality, results from the tests are collected and transmitted back to the diagnostic center. He thus teaches test logic is tested using the test routine under control of the microprocessor.

4. As per claim 2, With reference to a port is a parallel port, a serial port, a USB port or a JTAG port. Jacobson teaches at (col. 4, lines 55-57).

5. As per claims 3 & 4, With reference to memory is part of the programmable logic. Jacobson teaches at (col. 5, lines 25-28, Fig. 3).

6. As per claim 5, With reference to the microprocessor includes an analysis routine. Jacobson teaches at (col. 4, lines 25-30).

7. As per claim 6, With reference to the microprocessor includes control routine for controlling execution of the test routine. Jacobson teaches at (col. 5, lines 51-54).

8. As per claim 7, Jacobson substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 3, lines 38-40) a diagnostic microcontroller that initiates diagnostic testes on the programmable logic device (See Fig. 1) . He thus teaches a programmable logic device comprising a programmable logic that includes test logic, a port, and a hard-coded microprocessor in communication with the programmable logic. He also teaches (col. 3, lines 50-53) diagnostic microcontroller initiates diagnostic tests on the programmable logic device to test its functionality, results from the tests are collected and transmitted back to the diagnostic center. He thus teaches test logic is tested using the test routine under control of the microprocessor.

9. As per claim 8, With reference to a port is a parallel port, a serial port, a USB port or a JTAG port. Jacobson teaches at (col. 4, lines 55-57).

10. As per claims 9 & 10, With reference to memory is part of the programmable logic. Jacobson teaches at (col. 5, lines 25-28, Fig. 3).

11. As per claim 11, With reference to the microprocessor includes an analysis routine. Jacobson teaches at (col. 4, lines 25-30).

12. As per claim 12, With reference to the microprocessor includes control routine for controlling execution of the test routine. Jacobson teaches at (col. 5, lines 51-54).

13. As per claim 13, Jacobson substantially teaches the claimed invention as disclosed related to claim 1 above. With reference to PLD that includes programmable logic, an embedded microprocessor and associated memory. Jacobson teaches (col. 3, lines 38-40, and See fig. 2 & 3). With reference to downloading to the memory a test routine. He teaches at (col. 3, 47-50). With reference to executing the test routine under control of the microprocessor to test the programmable logic and sending results to a test system external. He teaches (col. 3, lines 38-40) a diagnostic microcontroller that initiates diagnostic testes on the programmable logic device (See Fig. 1). He also teaches (col. 3, lines 50-53) diagnostic microcontroller initiates diagnostic tests on the programmable logic device to test its functionality, results from the tests are collected and transmitted back to the diagnostic center.

14. As per claim 14, With reference to downloading to the microprocessor a control routine for controlling execution of the test routine. Jacobson teaches at (col. 4, lines 47-50).

15. As per claim 15, With reference to the results are the raw data. Jacobson teaches at (col. 3, lines 53-55).

16. As per claim 16, With reference to downloading to the microprocessor an analysis routine for analyzing the data and executing the analysis routine to produce results. Jacobson teaches (col. 4, lines 10-13). With reference to executing the analysis routine to produce the results. Jacobson teaches (col. 3, lines 54-56).

17. As per claim 17, With reference to downloading to the microprocessor a compression routine for compressing the raw data from the test routine, and sending the compressed raw data as the results. Jacobson teaches (col. 11, lines 23-28).

18. As per claims 18 & 19, With reference to memory is part of the programmable logic. Jacobson teaches at (col. 5, lines 25-28, Fig. 3).

19. As per claim 20, Jacobson substantially teaches the claimed invention as disclosed related to claim 1 above. With reference to PLD that includes programmable logic, an embedded microprocessor and associated memory. Jacobson teaches (col. 3, lines 38-40, See fig. 2 & 3). With reference to downloading to the memory a test routine. He teaches at (col. 3, 47-50). With reference to executing the test routine under control of the microprocessor to test the programmable logic and sending results to a test system external. He teaches (col. 3, lines 38-40) a diagnostic microcontroller that initiates diagnostic testes on the programmable logic device (See Fig. 1). He also teaches (col. 3, lines 50-53) diagnostic microcontroller initiates diagnostic tests on the programmable logic device to test its functionality, results from the tests are collected and transmitted back to the diagnostic center.

20. As per claim 21, With reference to downloading to the microprocessor a control routine for controlling execution of the test routine. Jacobson teaches at (col. 4, lines 47-50).

21. As per claim 22, With reference to the results are the raw data. Jacobson teaches at (col. 3, lines 53-55).

22. As per claims 23 & 24, With reference to downloading to the microprocessor an analysis routine for analyzing the data and executing the analysis routine to produce results. Jacobson teaches (col. 11, lines 12-17). With reference to executing the analysis routine to produce results. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center.

23. As per claims 25 & 26, With reference to memory is part of the programmable logic.

Jacobson teaches at (col. 5, lines 25-28, Fig. 3).

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI